

Aditya Shevade

University of Southern California, Los Angeles (CA), 90007

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www.adityashevade.com

Education

University of Southern California

Los Angeles (CA)

Masters in Electrical Engineering, *Majoring in Digital VLSI and Computer Architecture*

Expected Graduation: Fall, 2011

- **GPA: 3.75/4.0**
- **Courses:** Computer Systems Organization, Computer Systems Architecture, MOS VLSI Circuit Design, VLSI System Design, Mathematical Foundations of VLSI CAD, Computer Networks

Walchand College of Engineering, Affiliated to Shivaji University, Kolhapur

Sangli, India

Bachelor of Engineering, *Electronics; First Class with Distinction*

- **Aggregate Percentage: 70.00%**
- **Major Courses:** Computer Organization, Digital Systems Design, VLSI (VHDL), Embedded Systems (8085/86/51)

Work Experience

ASIC Design Intern at Advanced Micro Devices, Sunnyvale (CA)

June 2011 – August 2011

- Worked in the GPU ASIC design verification team – power management unit
- Wrote and debugged tests on power gating, DMA controller, firmware, GPIO, ROM
- Wrote script to manage regressions running across various projects
- Helped manage and clean up the amount of disk space used for all projects on front end design side

Freelance Author, Linux Magazines

January 2009 – Present

Published over 15 articles in various Linux magazines such as,

- Linux Magazine
- Ubuntu User
- Linux for You
- Linux Format

Technical Skills

- **Hardware Description Languages:** Verilog, VHDL, System Verilog (Basics)
- **Electronic Design Tools:** Verdi, Cadence Virtuoso, Xilinx ISE, ModelSim, Proteus, Protel, kSimus
- **Microprocessor/Controllers:** MIPS, AVR, 8051/85/86
- **Programming/Scripting Languages:** C, C++, Python, Bash, HTML, CSS, PHP(Basics), SQL, Perl
- **Operating Systems:** GNU/Linux, Unix, BSD, Windows (User Space)

Projects

Computer Architecture

- Design and analysis of super-scalar MIPS processor core based on comparison of various machine widths using SuperScalar and Cacti software and improvement of the same to get optimum performance across various benchmarks
- Implemented a 5 stage pipelined MIPS based processor core in Verilog; the processor had a full forwarding unit, internally forwarding register file, hazard detection unit and a non-vectored interrupt source
- Implemented a simplified multi-cycle MIPS core in Verilog which was later used as the base machine for the pipelined core

VLSI Projects

All projects done under 100nm technology using Cadence, Virtuoso

- Implemented layout of 16 bit motion vector estimator using SRAMs, absolute difference circuit and accumulators; the circuit was pipelined to achieve higher frequencies
- Implemented layout of 16 bit & 18 bit Ladner-Fischer adder after comparing it with Sklansky Adder on schematic level converted the 16 bit adder to a subtracter with logic synthesis in the same footprint
- Implemented layout of 256 bit (16X16) SRAM with the read/write circuitry, row decoder and sense amplifiers
- Implemented layout of 8 bit Baugh-Wooley multiplier
- Implemented layout of 12 bit Carry Select Adder (CSA)
- Implemented a simplified sequence detector neural network

Verilog/VHDL

- Implemented an 8 source programmable interrupt controller with polling and programmable priority modes (Verilog)
- Working on implementation of XR16L788 clone on Spartan 3E (Part of a peripheral chip) (Verilog)
- Implemented various circuits such as ALU, FIFO, Multiplier Algorithms (Verilog)
- Implemented various combinational and sequential circuits as course projects (VHDL)

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Microprocessor / Microcontroller Projects

- Analyzed motion of a body in free space by measuring its 6DoF parameters using MEMS sensors, ZigBEE communication module and an AVR processor with Arduino bootloader (*Senior Thesis*)
- Designed a single player Tic-Tac-Toe game on an AVR controller
- Designed a solar follower to be used with solar panel (8085)
- Built a real time clock with LCD display and binary outputs (AVR/8051)

Software Projects

- Developed a new algorithm for symmetric key encryption; currently working on cryptanalysis and implementation of the same in hardware (*Work in Progress*)
- Various software projects from website development and maintenance to android application development